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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/756,756	KIMURA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2008 and 18 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,12 and 81-91* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12 and 81-91* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/25/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Election/Restrictions

4. ***Applicant's election of Species 1 (claims 11, 12, and 81-91; fig. 3A; pages 9-10 of the specification)*** in the reply filed on *15 December 2008* is acknowledged and appreciated.

Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 12 and 85-91 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 85 recites the limitation "***the current source circuit***" (line 4). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art which of the earlier claimed "*a plurality of pairs of current source circuits*" (claim 11, line 3) and/or "*one pair of current source circuits*" (claim 11, line 9) this limitation is intended to refer to.

9. Claim 86 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a first current source circuit***" (claim 86, line 2); "***a pair of current source circuits***" (claim 86, line 2); "***a second current source circuit***" (claim 86, line 3); "***the current source circuit***" (claim 85, line 4); "***a plurality of pairs of current source circuits***" (claim 11, line 3); and "***one pair of current source circuits***" (claim 11, line 9). For example:

It would be unclear to one having ordinary skill in the art whether the above limitations are intended to be identical to, or distinct from, one another.

An omitted structural cooperative relationship results from the claimed subject matter: "***when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode***" (claim 86, line 5). For example:

It would be unclear to one having ordinary skill in the art how *the second current source circuit* can simultaneously operate in both the *set mode* and the *output mode*.

10. Claim 87 recites the limitation "***the current source circuit***" (line 4). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art which of the earlier claimed "*a plurality of pairs of current source circuits*" (claim 12, line 4); "*a particular pair of current*

source circuits" (claim 12, line 12); and/or "*one pair of current source circuits*" (claim 12, line 14) this limitation is intended to refer to.

11. Claim 88 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a first current source circuit***" (claim 88, line 2); "***a pair of current source circuits***" (claim 88, line 2); "***a second current source circuit***" (claim 88, line 3); "***the current source circuit***" (claim 87, line 4); "***a plurality of pairs of current source circuits***" (claim 12, line 4); "***a particular pair of current source circuits***" (claim 12, line 12); and "***one pair of current source circuits***" (claim 12, line 14). For example:

It would be unclear to one having ordinary skill in the art whether the above limitations are intended to be identical to, or distinct from, one another.

An omitted structural cooperative relationship results from the claimed subject matter: "***when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode***" (claim 88, line 5). For example:

It would be unclear to one having ordinary skill in the art how *the second current source circuit* can simultaneously operate in both the *set mode* and the *output mode*.

12. Claim 89 is amenable to two or more plausible claim constructions.

The use of the phrase "***the third switch***" renders the claim indefinite.

The claimed "***the third switch***" is amenable to two plausible definitions.

Based on the description provided in the Specification, "***the third switch***" could be interpreted to mean:

(a) Figure 9's switch (906) -- Due to claim 89 reciting "*the third switch is configured to select a second current source circuit of the particular pair of current source circuits*" (line 5) and "*the third switch is configured to select the first current source circuit of the particular pair of current source circuits*" (line 7).

(b) Figure 9's switch (905) -- Due to claim 12 reciting "*first and second switches are configured to be controlled by a latch pulse*" (line 18).

Thus, neither the Specification, nor the claims, nor the ordinary meanings of the words provides any guidance as to what Applicant intends to cover with this claim language.

Due to the ambiguity as to what is intended by the claimed "***the third switch***" and the fact that this claim element is amenable to two or more plausible claim constructions, this claim is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicant considers to be the invention.

See Ex parte Miyazaki (BPAI Precedential 19 November 2008).

13. Figure 9's switches (906 and 907) are "*configured to be controlled by a latch pulse*" -- suggesting that the claimed "*first switch*" (claim 12, line 7) is switch (906) and the claimed "*second switch*" (claim 12, line 9) is switch (907).

This leaves only switch (905) to be the claimed "*third switch*" (claim 89, line 1)

However, switch (905) is not "*configured to select a second current source circuit of the particular pair of current source circuits*" nor "*configured to select the first current source circuit of the particular pair of current source circuits*" (claim 89, lines 5 & 7).

Therefore, dependent claim 89 throws into question the scope and limitations of independent claim 12.

14. Claim 90 recites the limitation "***the current source circuit***" (line 4). There is insufficient antecedent basis for this limitation in the claim. For example:

It would be unclear to one having ordinary skill in the art which of the earlier claimed "*a plurality of current source circuits*" (claim 81, line 2) this limitation is intended to refer to.

15. Claim 91 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a first current source circuit***" (claim 91, line 2); "***a pair of current source circuits***" (claim 91, line 2); "***a second current source circuit***" (claim 91, line 3); "***the current source circuit***" (claim 90, line 4); and "***a plurality of current source circuits***" (claim 81, line 2). For example:

It would be unclear to one having ordinary skill in the art whether the above limitations are intended to be identical to, or distinct from, one another.

An omitted structural cooperative relationship results from the claimed subject matter: "***when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode***" (claim 91, line 5). For example:

It would be unclear to one having ordinary skill in the art how *the second current source circuit* can simultaneously operate in both the *set mode* and the *output mode*.

16. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 11, 12, and 81 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Koyama et al (US 2001/0048408 A1)***.

Regarding claim 11, Koyama discloses a signal line driver circuit [Fig. 1] comprising:

a shift register [Fig. 1; First - Third Shift Registers];

a latch circuit [Fig. 1; LAT Portion], electrically connected to the shift register, comprising a plurality of pairs of current source circuits [Fig. 5B], wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] depending on a value of the signal current (see Pages 5-6; Paragraphs 88-89 -- wherein an output current value will at least partially be dependent on the presence/absence of an input signal current); and

a changing over circuit [Fig. 1; 10a] electrically connected to the plurality of pairs of current source circuits and a plurality of signal lines [Fig. 1; S001 - S640],

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines, and

wherein the shift register is configured to output the set signal (see Page 3; Paragraphs 50-53).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 11; furthermore, Koyama discloses a signal line driver circuit [Fig. 6] comprising:

a shift register [Fig. 6; First - Third Shift Registers]; a latch circuit [Fig. 1; Latch Circuit Portion], electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits [Fig. 5B], wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] depending on a value of the signal current (see Pages 5-6; Paragraphs 88-89 -- wherein an output current value will at least partially be dependent on the presence/absence of an input signal current);

a first switch (see Fig. 5B) provided between the shift register and each of the plurality of pairs of current source circuits (see Pages 5-6; Paragraphs 88-89); and

a second switch [Fig. 6; 20] (see Page 6; Paragraphs 90-92), and

a changing over circuit [Fig. 6; 10c] electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines,

wherein the changing over circuit is electrically connected [e.g., Fig. 6: via Latch Circuit Portion, L001, BPC, PW-001, 20, DA-001, 10c] to a particular pair of current source circuits through the second switch (see Page 6; Paragraphs 92-93),

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines,

wherein the shift register is configured to output the set signal, and

wherein the first and second switches are configured to be controlled by a latch pulse [Fig. 1; LP] (see Page 3; Paragraphs 50-53).

Regarding claim 81, this claim is rejected by the reasoning applied in rejecting claims 11 and 12; furthermore, Koyama discloses a signal line driver circuit [Fig. 1] comprising:

a plurality of current source circuits [Fig. 5B], wherein each of the plurality of current source circuits is configured to be supplied with a first current [Fig. 5B; Input] and to supply a second current [Fig. 5B; Output], and wherein a value of the second current depends on a value of the first current (see Pages 5-6; Paragraphs 88-89 -- wherein a second/output current value will at least partially be dependent on the presence/absence of a first/input signal current);

a plurality of signal lines [Fig. 1; S001 - S640]; and

a selector circuit [Fig. 1; 10a] electrically connected between the plurality of current source circuits and the plurality of signal lines, wherein the selector circuit is configured to select one of the plurality of signal lines to which the second current is supplied (see Page 3; Paragraphs 50-53).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 82-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Koyama et al (US 2001/0048408 A1)*** in view of ***Akimoto et al (US 6,850,216 B2)***.

Regarding claim 82, Koyama discloses each of the current source circuits [Fig. 5B; transistor pairs] includes at least one transistor having a gate, and

controlling a voltage [Fig. 5B; Control Signals 1 & 2] applied to the gate of the transistor (see Page 3; Paragraphs 50-53).

One having ordinary skill in the art would recognize Koyama's gate controlling voltages [Fig. 5B; Control Signals 1 & 2] would necessarily and inherently be set via at least one switch -- otherwise the control signals would remain constant and provide no "control" whatsoever over Koyama's SRAM circuit.

However, should the applicants prove the Koyama reference neglects to teach such switch control with sufficient specificity; Akimoto does disclose current source circuits including at least one switch [Fig. 27; 201 & 202] and at least one transistor [Fig. 27; 205 & 206] having a

gate, with the switch being connected to control a voltage applied to the gate of the transistor (see Column 1, Lines 10-53).

Koyama and Akimoto are analogous art, because they are from the shared inventive field of controlling SRAM type circuitry.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Akimoto's switches to set Koyama's controlling voltages [Koyama: Fig. 5B; Control Signals 1 & 2], because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predicable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 83, this claim is rejected by the reasoning applied in rejecting claim 82.

Regarding claim 84, this claim is rejected by the reasoning applied in rejecting claim 82.

Regarding claim 85, Koyama discloses each of the current source circuits includes at least one capacitor [*e.g., Fig. 5B: gate capacitance of each transistor -- wherein the instant invention states, "capacitor 309 may be substituted by a gate capacitance of a transistor"*] and at least one transistor, and

operates in a set mode [*e.g., off*] or an output mode [*e.g., on*] depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged (*see the entire document, including Pages 5-6; Paragraphs 88-89*).

Koyama also discloses each of the current source circuits includes at least one capacitor [*e.g., Fig. 5C: illustrated capacitor*] and at least one transistor, and

operates in a set mode or an output mode depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged (*see the entire document, including Pages 5-6; Paragraphs 88-89*).

Akimoto also discloses each of the current source circuits includes at least one capacitor [*e.g., Fig. 27: gate capacitance of each transistor 201, 202, 205, 206 -- wherein the instant invention states, "capacitor 309 may be substituted by a gate capacitance of a transistor"*] and at least one transistor, and

operates in a set mode [*e.g., off*] or an output mode [*e.g., on*] depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged (*see the entire document, including Column 1, Lines 10-53*).

Regarding claim 86, Koyama discloses when a first current source circuit [*e.g., Fig. 5B: first transistor*] of a pair of current source circuits is operating in the set mode,

a second current source circuit [*e.g., Fig. 5B: second transistor*] of the pair of current source circuits is operating in the output mode; and

when the second current source circuit of the pair of current source circuits is operating in the set mode,

the second current source circuit of the pair of current source circuits is operating in the output mode (*see the entire document, including Pages 5-6; Paragraphs 88-89*).

Akimoto also discloses when a first current source circuit [*e.g., Fig. 27: 205*] of a pair of current source circuits is operating in the set mode,

a second current source circuit [*e.g., Fig. 5B: 206*] of the pair of current source circuits is operating in the output mode; and

when the second current source circuit of the pair of current source circuits is operating in the set mode,

the second current source circuit of the pair of current source circuits is operating in the output mode (*see the entire document, including Column 1, Lines 10-53*).

Regarding claim 87, this claim is rejected by the reasoning applied in rejecting claim 85.

Regarding claim 88, this claim is rejected by the reasoning applied in rejecting claim 86.

Regarding claim 89, Akimoto discloses a third switch [*e.g., Fig. 27: 201*] connected between the particular pair of current source circuits [*e.g., Fig. 27: 203-206*] and the signal current [*e.g., Fig. 27: 212, 213*], wherein

the second and third switches are controlled such that,

when the second switch [*e.g., Fig. 27: 202*] is configured to select a first current source circuit [*e.g., Fig. 27: 205*] of the particular pair of current source circuits,

the third switch [*e.g., Fig. 27: 201*] is configured to select a second current source circuit [*e.g., Fig. 27: 206*] of the particular pair of current source circuits, and,

when the second switch is configured to select the second current source circuit of the particular pair of current source circuits,

the third switch is configured to select the first current source circuit of the particular pair of current source circuits (see Column 1, Lines 10-53).

Regarding claim 90, this claim is rejected by the reasoning applied in rejecting claim 85.

Regarding claim 91, this claim is rejected by the reasoning applied in rejecting claim 86.

Response to Arguments

22. Applicant's arguments filed 18 April 2008 have been fully considered but they are not persuasive.

The Applicant contends, "*Koyama does not describe or suggest pairs of current source circuits such as are recited in claim 11. In particular, Koyama does not describe or suggest that a pair 'of current source circuits is configured to receive a set signal and a signal current, and to control an output current value depending on a value of the signal current.' The rejection points to Fig. 5B of Koyama and, in particular, the pair of transistors that receive 'CONTROL SIGNAL 1' and 'CONTROL SIGNAL 2,' as corresponding to a pair of current sources. However, each of these transistors cannot be said to be a current source circuit. Rather, these transistors merely serve to either connect the 'INPUT' voltage with the input to the latch produced by the two inverters, or to isolate the 'INPUT' voltage from the input to the latch*" (see Pages 7-8 of the Response filed 18 April 2008). However, the examiner respectfully disagrees.

Koyama discloses a plurality of pairs of current source circuits [Fig. 5B; transistor pair], wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] depending on a value of the signal current (see Pages 5-6; Paragraphs 88-89 -- wherein an output current value will at least partially be dependent on the presence/absence of an input signal current).

The applicants argue, "*the output current of Koyama's SRAM circuit will depend primarily on the input impedance of devices to which the output of Koyama's SRAM circuit is connected, and will not be controlled based on a value of a received signal current*" (see Page 18

of the 'Amendment in Reply to Action of August 9, 2007' filed 29 October 2007). However, again the examiner respectfully disagrees.

Ohm's law states that the electrical current passing through a conductor between two points is proportional to the potential difference (i.e. voltage drop or voltage) across the two points, and inversely proportional to the resistance between them (i.e., $\boldsymbol{I = V / R}$). Even if arguably resistance varies across Koyama's SRAM circuit in Figure 5B; the applicants themselves concede Koyama's *"output potential[is] based on an input potential received at a particular time*" (see Page 18 of the 'Amendment in Reply to Action of August 9, 2007' filed 29 October 2007).

Therefore, Koyama's output current will inherently be (at least partially) dependent upon the presence or absence of input current/voltage. As such, Koyama's SRAM circuit would indeed control an output current [Fig. 5B; Output] depending on an input signal current [Fig. 5B; Input], as instantly claimed.

Perhaps the simplest example of such an input-to-output current signal correspondence is that absent an input current signal, no output current signal will exist in Koyama's SRAM circuit. However, once an input current signal is applied to Koyama's current source circuit [Fig. 5B; transistor pair], and control signals 1 and 2 are switched turn the corresponding transistors on, a current signal will be output.

The Applicant contends, "*The rejection indicates that the pairs of current sources and the first switch are shown in Fig. 5B of Koyama. However, in order for this to be the case, the first switch, which needs to be between the shift register and the pairs of current sources, would need*

to be the pair of transistors that receive 'CONTROL SIGNAL 1' and 'CONTROL SIGNAL 2,' in which case the two inverters that make up the latch would need to be the pairs of current sources. However, claim 12 further requires the current sources to receive a set signal from the shift register and a signal current, and the only signal received by the inverters is the output of the two transistors. Accordingly, the inverters cannot be the pairs of current sources and Fig. 513 does not describe or suggest both the first switch and the pairs of current sources. Accordingly, for at least this additional reason, the rejection of claim 12 should be withdrawn" (see Page 8 of the Response filed 18 April 2008). However, the examiner respectfully disagrees.

Koyama discloses that the 'Latch Circuit Portion' comprises a plurality of storage circuits (LAT) organized in groups of three, therefore, for example:

Koyama discloses a signal line driver circuit [*Fig. 1*] comprising:

a shift register [*Fig. 1; First, Second, Third Shift Registers*];

a latch circuit [*Fig. 1; Latch Circuit Portion*], electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits [*Figs. 1, 5B: both switches in each third LAT*], wherein each of the plurality of pairs of current source circuits is configured to receive a set signal [*Fig. 5B; Control Signals 1 & 2*] and a signal current [*Fig. 5B; Input*], and to control an output current value [*Fig. 5B; Output*] depending on a value of the signal current (*see Pages 5-6; Paragraphs 88-89 -- wherein an output current value will at least partially be dependent on the presence/absence of an input signal current*);

a first switch [*Figs. 3, 5B: first switch in the second LAT*] provided between the shift register and each of the plurality of pairs of current source circuits; and

a second switch [*Figs. 3, 5B: second switch in the first LAT*], and

a changing over circuit [*Fig. 1; 10a*] electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines [*Fig. 1: S*],

wherein the changing over circuit is electrically connected [*Fig. 1: via Latch Circuit Portion, L001, DAC, 10a*] to a particular pair of current source circuits through the second switch,

wherein the changing over circuit is configured to select one pair of current source circuits from the plurality of pairs of current source circuits for electrically connecting to each of the plurality of signal lines,

wherein the shift register is configured to output the set signal, and

wherein the first and second switches are configured to be controlled by a latch pulse [*Fig. 1; LP*] (see Page 3; Paragraphs 50-53).

The Applicant contends, "*Nor does Koyama describe or suggest a second switch through which the changing over circuit is electrically connected to a particular pair of current source circuits. The rejection indicates that the second switch is provided by an analog switch 20 of Fig. 6. However, while an analog switch 20 provides an output to a signal line selecting circuit 10c, which the rejection equates with the changing over circuit, the analog switch 20 is isolated from the latch circuit portion by the bit comparison pulse-width converter circuit (BPC), such that the analog switch cannot connect the signal line selecting circuit 10c with a pair of current source*

circuits of the latch circuit. Accordingly, for at least this additional reason, the rejection of claim 12 should be withdrawn" (see Page 9 of the Response filed 18 April 2008). However, the examiner respectfully disagrees.

Koyama discloses a changing over circuit [Fig. 6; 10c] electrically connected between the plurality of pairs of current source circuits and a plurality of signal lines,

wherein the changing over circuit is electrically connected [e.g., Fig. 6: via Latch Circuit Portion, L001, BPC, PW-001, 20, DA-001, 10c] to a particular pair of current source circuits through the second switch (see Page 6; Paragraphs 92-93),

Applicant's arguments with respect to claims 11, 12, 82, 83, and 85-91 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
13 March 2009